

Individual Laser Control on T-BERD

- How does this work?
 - Address A013 controls the network lanes = Lasers
 - SR10 has 10 network lanes
 - Controlled by 10 bits
 - Bit set to 0 means laser on
 - Set A013 to 0 and 10 lasers on
 - Set A013 to 1 and laser 1 is off
 - Set A013 to 8 and laser 4 is off
 - Set A013 to FF and lasers 1 through 8 are off
 - Set A013 to 3FF and all lasers are off
 - Set A013 to 0 and we're back to all lasers on

P1: 100GigE Layer 2 Traffic Term Level (dBm) 9.6 Freq Dev (ppm) 0.0 Running 22s

Setup

Restart

SAM-Complete

Enhanced RFC 2544

Quick Check

Ethernet Payload Traffic 512 Test Mode Frame Size

- Summary
- Ethernet
 - Signal Present
 - Sync Acquired
 - Link Active
 - Marker Lock
 - Loss Of Align.
 - HI BER
 - Frame Detect
 - ATP Detect
 - Pattern Sync
 - VLAN Frame Detect
 - SVLAN Frame Detect
 - Local Fault Detect
 - Remote Fault Detect
 - History

Interface Lambda FPGA All

CFP2 Per Lane Signal Present

Lambda #1	ON
Lambda #2	ON
Lambda #3	ON
Lambda #4	ON
Lambda #5	ON
Lambda #6	ON
Lambda #7	ON
Lambda #8	ON
Lambda #9	ON
Lambda #10	ON

CFP2 Rx Level per Lambda (dBm)

Lambda #1	-0.3
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FPGA All

Line1 FPGA0 Name cmb_rev2_f1_eth40g100g.rbf

Line1 FPGA0 Date 2014/05/04

Line1 FPGA0 Time 01:00:50

Laser Actions Service Disruption Alarms Errors Faults

Traffic Started

Loop Up Loop Down LLB Pause Frame Insert



Interface Ethernet Traffic Filters Timed Test

Connector Signal Bit Skew Injection Physical Layer Network Visibility

Connector CFP2

CFP2 Expert Configuration Engineering MDIO I2C

Vendor	AVAGO	Power Class	<= 9 W
Vendor PN	AFBR-8420Z	Rx Power Level Type	Average Power
Vendor SN	FD46F001U	Rx Max Lambda Power (dBm)	3.39988
Date Code	20131115	Tx Max Lambda Power (dBm)	3.39988
Lot Code		# of Active Fibers	10
HW / SW Version#	3.13 / 1.0	Wavelengths per Fiber	0
MSA HW Spec. Rev#	1.0	Diagnosis Byte	12
MSA Mgmt. I/F Rev#	2.2	WL per Fiber Range (nm)	0 - 0
Module ID	CFP2	Max Ntwk Lane Bit Rate (Gbps)	11.2000
Rates Supported			
Transceiver	100GE MMF 100m		



Interface Ethernet Traffic Filters Timed Test

Connector Signal Bit Skew Injection Physical Layer Network Visibility

Connector CFP2

CFP2 Expert Configuration Engineering MDIO I2C

Peek DevType 0001 Peek PhyAddr 0001

Peek RegAddr A013 Peek Value 0x01

Peek Peek Success 1

Poke DevType 0001 Poke PhyAddr 0001

Poke RegAddr A013 Poke Value 0001

Poke Poke Success 1



P1: 100GigE Layer 2 Traffic Term

Level (dBm) 9.2
Freq Dev (ppm) ---



Running

1m:06s



Ethernet Payload

Traffic

512

Test Mode

Frame Size

- Summary
- Ethernet
- Signal Present
- Sync Acquired
- Link Active
- Marker Lock
- Loss Of Align.
- HI BER
- Frame Detect
- ATP Detect
- Pattern Sync
- VLAN Frame Detect
- SVLAN Frame Detect
- Local Fault Detect
- Remote Fault Detect
- History

Interface Lambda

CFP2 Per Lane Signal Present

Lambda #1	OFF
Lambda #2	ON
Lambda #3	ON
Lambda #4	ON
Lambda #5	ON
Lambda #6	ON
Lambda #7	ON
Lambda #8	ON
Lambda #9	ON
Lambda #10	ON

CFP2 Rx Level per Lambda (dBm)

Lambda #1	Unavailable
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FPGA All

Line1 FPGA0 Name
cmb_rev2_f1_eth40g100g.rbf

Line1 FPGA0 Date
2014/05/04

Line1 FPGA0 Time
01:00:50

Laser

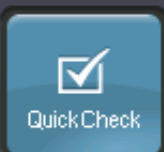
Actions

Service Disruption

Alarms

Errors

Faults





Interface Ethernet Traffic Filters Timed Test

Connector Signal Bit Skew Injection Physical Layer Network Visibility

Connector CFP2

CFP2 Expert Configuration Engineering MDIO I2C

Peek DevType 0001 Peek PhyAddr 0001

Peek RegAddr A013 Peek Value 0x08

Peek Peek Success 1

Poke DevType 0001 Poke PhyAddr 0001

Poke RegAddr A013 Poke Value 0008

Poke Poke Success 1



P1: 100GigE Layer 2 Traffic Term

Level (dBm)

9.0

▶ Running

1m:59s



Setup



Restart

Ethernet

Payload

Traffic

512

Test Mode

Frame Size

- Summary
- Ethernet
- Signal Present
- Sync Acquired
- Link Active
- Marker Lock
- Loss Of Align.
- HI BER
- Frame Detect
- ATP Detect
- Pattern Sync
- VLAN Frame Detect
- SVLAN Frame Detect
- Local Fault Detect
- Remote Fault Detect
- History

Interface

Lambda

FPGA

All

CFP2 Per Lane Signal Present

Lambda #1	ON
Lambda #2	ON
Lambda #3	ON
Lambda #4	OFF
Lambda #5	ON
Lambda #6	ON
Lambda #7	ON
Lambda #8	ON
Lambda #9	ON
Lambda #10	ON

CFP2 Rx Level per Lambda (dBm)

Lambda #1	-0.5
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Line1 FPGA0 Name

cmb_rev2_f1_eth40g100g.rbf

Line1 FPGA0 Date

2014/05/04

Line1 FPGA0 Time

01:00:50



SAM-Complete



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QuickCheck

Laser

Actions

Service Disruption

Alarms

Errors

Faults

Traffic Started

Loop Up

Loop Down

LLB

Pause Frame Insert



Interface Ethernet Traffic Filters Timed Test

Connector Signal Bit Skew Injection Physical Layer Network Visibility

Connector CFP2

CFP2 Expert Configuration Engineering MDIO I2C

Peek DevType 0001 Peek PhyAddr 0001

Peek RegAddr A013 Peek Value 0xFF

Peek Peek Success 1

Poke DevType 0001 Poke PhyAddr 0001

Poke RegAddr A013 Poke Value 00FF

Poke Poke Success 1

Select Test View Reports Tools Help P1: 100GigE Layer 2 Traffic Term

P1: 100GigE Layer 2 Traffic Term Level (dBm) 2.6 Running 4m:52s

Freq Dev (ppm) ---

Ethernet Payload

Traffic 512

Test Mode Frame Size

- Summary
- Ethernet
 - Signal Present
 - Sync Acquired
 - Link Active
 - Marker Lock
 - Loss Of Align.
 - HI BER
 - Frame Detect
 - ATP Detect
 - Pattern Sync
 - VLAN Frame Detect
 - SVLAN Frame Detect
 - Local Fault Detect
 - Remote Fault Detect
- History

Interface Lambda

CFP2 Per Lane Signal Present

Lambda #1	OFF
Lambda #2	OFF
Lambda #3	OFF
Lambda #4	OFF
Lambda #5	OFF
Lambda #6	OFF
Lambda #7	OFF
Lambda #8	OFF
Lambda #9	ON
Lambda #10	ON

CFP2 Rx Level per Lambda (dBm)

Lambda #1	Unavailable
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FPGA All

Line1 FPGA0 Name cmb_rev2_f1_eth40g100g.rbf

Line1 FPGA0 Date 2014/05/04

Line1 FPGA0 Time 01:00:50

Setup

Restart

SAM-Complete

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QuickCheck

Laser Actions Service Disruption Alarms Errors Faults

Traffic Started Loop Up Loop Down LLB Pause Frame Insert



Interface Ethernet Traffic Filters Timed Test

Connector Signal Bit Skew Injection Physical Layer Network Visibility

Connector CFP2

CFP2 Expert Configuration Engineering MDIO I2C

Peek DevType 0001 Peek PhyAddr 0001

Peek RegAddr A013 Peek Value 0x3FF

Peek Peek Success 1

Poke DevType 0001 Poke PhyAddr 0001

Poke RegAddr A013 Poke Value 03FF

Poke Poke Success 1

P1: 100GigE Layer 2 Traffic Term

Level (dBm) ---

▶ Running

5m:36s

Setup

Restart

Ethernet

Payload

Traffic

512

Test Mode

Frame Size

- Summary
- Ethernet
- Signal Present
- Sync Acquired
- Link Active
- Marker Lock
- Loss Of Align.
- HI BER
- Frame Detect
- ATP Detect
- Pattern Sync
- VLAN Frame Detect
- SVLAN Frame Detect
- Local Fault Detect
- Remote Fault Detect
- History

Interface Lambda

CFP2 Per Lane Signal Present

Lambda #1	OFF
Lambda #2	OFF
Lambda #3	OFF
Lambda #4	OFF
Lambda #5	OFF
Lambda #6	OFF
Lambda #7	OFF
Lambda #8	OFF
Lambda #9	OFF
Lambda #10	OFF

CFP2 Rx Level per Lambda (dBm)

Lambda #1	Unavailable
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FPGA All

Line1 FPGA0 Name
cmb_rev2_f1_eth40g100g.rbf

Line1 FPGA0 Date
2014/05/04

Line1 FPGA0 Time
01:00:50

SAM-Complete

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Quick Check

Laser Actions Service Disruption Alarms Errors Faults

Traffic Started | Loop Up | Loop Down | LLB | Pause Frame Insert



Interface Ethernet Traffic Filters Timed Test

Connector Signal Bit Skew Injection Physical Layer Network Visibility

Connector CFP2

CFP2 Expert Configuration Engineering MDIO I2C

Peek DevType 0001 Peek PhyAddr 0001

Peek RegAddr A013 Peek Value 0x00

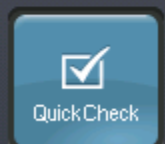
Peek Peek Success 1

Poke DevType 0001 Poke PhyAddr 0001

Poke RegAddr A013 Poke Value 0000

Poke Poke Success 1

P1: 100GigE Layer 2 Traffic Term Level (dBm) 9.6 Running 6m:27s
Freq Dev (ppm) 0.0



Ethernet Payload
Traffic 512
Test Mode Frame Size

- Summary
- Ethernet
 - Signal Present
 - Sync Acquired
 - Link Active
 - Marker Lock
 - Loss Of Align.
 - HI BER
 - Frame Detect
 - ATP Detect
 - Pattern Sync
 - VLAN Frame Detect
 - SVLAN Frame Detect
 - Local Fault Detect
 - Remote Fault Detect
- History

Interface	Lambda
CFP2 Per Lane Signal Present	
Lambda #1	ON
Lambda #2	ON
Lambda #3	ON
Lambda #4	ON
Lambda #5	ON
Lambda #6	ON
Lambda #7	ON
Lambda #8	ON
Lambda #9	ON
Lambda #10	ON
CFP2 Rx Level per Lambda (dBm)	
Lambda #1	-0.6

FPGA All
Line1 FPGA0 Name
cmb_rev2_f1_eth40g100g.rbf
Line1 FPGA0 Date 2014/05/04
Line1 FPGA0 Time 01:00:50

Laser Actions Service Disruption Alarms Errors Faults

Traffic Started | Loop Up | Loop Down | LLB | Pause Frame Insert

P1: 100GigE Layer 2 Traffic Term Level (dBm) 9.6 Running 6s
Freq Dev (ppm) ---

Ethernet Payload
Traffic 512
Test Mode Frame Size

- Summary
- Ethernet
 - Signal Present
 - Sync Acquired
 - Link Active
 - Marker Lock
 - Loss Of Align.
 - HI BER
 - Frame Detect
 - ATP Detect
 - Pattern Sync
 - VLAN Frame Detect
 - SVLAN Frame Detect
 - Local Fault Detect
 - Remote Fault Detect
- History

Interface	Lambda
CFP2 Per Lane Signal Present	
Lambda #1	ON
Lambda #2	ON
Lambda #3	ON
Lambda #4	ON
Lambda #5	ON
Lambda #6	ON
Lambda #7	ON
Lambda #8	ON
Lambda #9	ON
Lambda #10	ON
CFP2 Rx Level per Lambda (dBm)	
Lambda #1	-0.6

FPGA	All
Line1 FPGA0 Name	
cmb_rev2_f1_eth40g100g.rbf	
Line1 FPGA0 Date	
2014/05/04	
Line1 FPGA0 Time	
01:00:50	

Setup

Restart

SAM-Complete

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QuickCheck

Laser Actions Service Disruption Alarms Errors Faults

Traffic Started | Loop Up | Loop Down | LLB | Pause Frame Insert